TDI "ULDB MODE"
System Functional Test
Procedure

Version 1.1

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<u>Signature Sheet</u>

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CHANGE INFORMATION PAGE

Version	Date	Description	Affected Pages
1.0	03/06/2000	Original.	all
1.1	03/14/2000	Added Sentence to briefly describe differences in version 1.0 and 1.1	Page 1: section 1.0
1.1	03/14/2000	Changed wait 2 minutes to wait 1 minute between measurements to shorten test time.	Pages 5-23
1.1	03/14/2000	Changed expected Latched FIFO status value to 0x00. The previous version had an incorrect value.	Page 5: section 3.3 step 5
1.1	03/14/2000	Changed the step number referenced for "Expected values" to correct step number.	Page 20 3.17 steps 9 and 10

1. Overview

This document describes the ULDB Mode System Functional Test (SFT) that is to be performed on every TDI card. The test exercises all functions of the TDI card in the ULDB mode. This version of the procedure differs from Version 1.0 in that "red-lines" encountered during prototype testing are incorporated and the wait times are lessened to shorten the test time.

1.1 Test Purpose

The purpose of this test is to demonstrate that all functions of the TDI board work properly. This test will be run in ambient and during the TDI thermal tests.

1.2 Test Organization

This test exercises the ULDB mode TDI board in 16 configurations. Each data source, encoding scheme and PCM discrete select mode is operated.

1.3 Applicable Documents

The following documents are applicable to this document:

Ultra Long Duration Balloon(ULDB) TDRSS Data Interface (TDI) Test Plan December,1999

Ultra Long Duration Balloon (ULDB) TDRSS Data Interface (TDI)
Interface Control Document   January, 2000

Electrostatic Discharge Control, NASA-STD-8739.7   December, 1997

1.4 Configuration Management

This document shall be managed by the ULDB TDI development team. Changes to this test procedure shall require the approval of the Ultra Long Duration (ULDB) TDRSS Data Interface (TDI) Product Development Lead.

During the execution of this test, typographical and procedural flow changes may be made at the discretion of the TDI Test Engineer. The changes will then be submitted for approval at the conclusion of the test.

After test execution, the completed test procedure shall be maintained by the TDI team as an "As Run" procedure.

1.5 Quality Assurance

This test will not be monitored by quality assurance. However, prior to the execution of this test, the test engineer shall verify the test configuration, test equipment calibration, documentation and ESD certification of test personnel. After this initial verification, testing shall commence. If anomalies are encountered during the execution of this test, the TDI Systems Engineer shall be notified. The execution of this test procedure shall be documented on a GSFC Work Order Authorization (WOA). Any anomalies shall be logged as a Non-Conformance Report (NCR) as per the GSFC QMS. At the conclusion of the test, the TDI Systems Engineer shall review the test results and approve any typographical changes or procedural flow deviations.

2. Test Setup

2.1 Test Personnel

This test shall be performed by one or more test conductors:

_____
Test Conductor # 1

_____
Test Conductor #2

2.2 Documentation Required

To commence testing, two documents shall be in place. First a signed copy of this test procedure is required. Second a GSFC WOA is in place.

This test procedure has been signed: Check_____

A GSFC WOA is in place.   WOA Number:_____

If this procedure is being run as part of another procedure record Event#
Of the WOA:
          EventNumber:_____ or Invoking Procedure Step Number_____
                                                             Check:_____

2.3 Equipment Required

The following equipment is required for this test. Refer to the test plan for configuration details.

If this procedure is being executed as a standalone procedure ie not part of another procedure, then the following shall be verified:

	Cal ID	Cal Date
PC-104 development system OR "flight like CDM"		
TDI Board		
Bit Sync with viterbi decoder		
HP 8015A Pulse Generator	_____	_____
Firebird 6000 Communications Analyzer	_____	_____
Phillips PM6680B High Resolution Prog Timer/Counter	_____	_____
ULDB TDI "Diagnostic Software"		

All required calibratable test gear is in calibration   Check:_____

2.4 Test Configuration

If this procedure is being executed as a "standalone procedure", ie not part of another procedure, then the following shall be verified.

The test set-up is configured as in Figure 2.4.   Check:_____

2.5 ESD Precautions:

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All TDI hardware shall be handled in compliance with NASA-STD-8739.7 for Electrostatic Discharge Control. All test personnel shall have current ESD certification. All test areas and benches shall also be ESD certified and test area shall be maintained between 30% and 70% humidity.

Wrist straps shall be worn at all times while either handling or within 3 feet of the TDI hardware. These wrist straps shall be verified for resistance at least 1 time each day. Non-static generating garments shall be worn by test personnel when within 3 feet of the TDI board.

If this procedure is being executed as a "standalone procedure" ie, not part of another procedure, then the following steps shall be performed.

Test facility is between 30% and 70% humidity.   Check:_____

Test personnel have ESD certification.   Check:_____

Wrist straps are functioning.   Check:_____

Non-static generating clothing is worn.   Check:_____

3. System Functional Test Procedure

3.1 Test Initialization

If this test is not part of a larger test, then

(1) Verify that the PC 104 development system or "flight like CDM" is powered off. Check:_____

(2) Verify that the TDI GSE rack is powered off.   Check:_____

(3) Record the serial number of the TDI board.   SN:_____   Check:_____

(4) Record the FPGA Silicon Signature Number: Sig Num:_____   Check:_____

(5) Verify that the TDI ULDB Mode select jumper is removed.   Check:_____

(6) Record TDI board IRQ and Base Address settings.
        IRQ: _____
        Base Addr:_____   Check:_____

(7) Verify that the GSE telemetry cable is connected to TDI connector P4   Check:_____

(8) Verify that the GSE Discrete Deck Select cable is connected to TDI connector P3 Check:_____

(9) Verify that the GSE test point cables are connected to TDI connectors P5 and P6 Check:_____

(10) Power the TDI GSE rack   Check:_____

(11) Verify the Bit Sync Stored format settings.

      a. Enter 130 on bit sync key-pad and verify
          Data Rate = 3.000*10**5
          Input Code = 0 (NRZ-L)
          FEC Code = 2 (BPSK-D)

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FEC Rate=1 (1/2)

b. Enter 131 on bit sync key-pad and verify
Data Rate = 1.500*10**5
Input Code = 0 (NRZ-L)
FEC Code = 0 (OFF)
FEC Rate= N/A

c. Enter 132 on bit sync key-pad and verify
Data Rate = 2.000*10**3
Input Code = 0 (NRZ-L)
FEC Code = 2 (BPSK-D)
FEC Rate = 1 (1/2)

d. Enter 133 on bit sync key-pad and verify
Data Rate = 1.000*10**3
Input Code = 0 (NRZ-L)
FEC Code = 0 (OFF)
FEC Rate = N/A

e. Enter 134 on bit sync key-pad and verify
Data Rate = 1.000*10**5
Input Code = 0 (NRZ-L)
FEC Code = 2 (BPSK-D)
FEC Rate = 1 (1/2)

f. Enter 135 on bit sync key-pad and verify
Data Rate = 5.000*10**4
Input Code = 0 (NRZ-L)
FEC Code = 0 (OFF)
FEC Rate = N/A

g. Enter 136 on bit sync key-pad and verify
Data Rate = 1.500*10**5
Input Code = 1(NRZ-M)
FEC Code = 0 (OFF)
FEC Rate = N/A

h. Enter 137 on bit sync key-pad and verify
Data Rate = 1.500*10**5
Input Code = 3 (BiO-L)
FEC Rate = 0 (OFF)
FEC Rate = N/A

Check:_____

(11) Power the PC 104 development system or the "flight-like CDM"   Check:_____

(12) Start the TDI diagnostic software   Check:_____
Verify FIFO LOAD MODE = Normal
Verify MISSION MODE=ULDB
If different, toggle the input to get the above settings

3.2 Hard Rest Verification Test

If this procedure is not being executed as a standalone procedure, but rather as part of a larger procedure which call for the execution of the SFT, then the following steps shall be performed:

(1) Read all registers and confirm their proper states at initial power up:
   a. Read I/O Port 0x00 and confirm = 0x00. Value read:_____
   b. Read I/O Port 0x01 and confirm = 0x09. Value read:_____
   c. Read I/O Port 0x02 and confirm = 0x00. Value read:_____
   d. Read I/O Port 0x03 and confirm = 0x00. Value read:_____

If any of the values read differ from the expected values, the test FAILS.

Check:_____
Circle:PASS/FAIL

3.3 BERT ENCODED 150KHZ PCMA Test

(1) Verify that PCM Discrete Deck A is selected by Reading I/O Port 0x01 and noting that the msb is zero. If not zero, the test failed.Reg Value:_____ Check:_____
Circle:PASS/FAIL

(2) Enter 130 on bit sync key-pad to configure bit sync as follows:
   Data Rate: 300Kbps (symbol rate)
   Input code: NRZ-L
   FEC Code:BPSK-D
   Rate: ½

Check:_____

(3) Configure Firebird 6000 for BERT Pattern 2047 and press RESTART   Check:_____

(4) Patch A1TLM to BS#1 S0 IN   Check:_____

(5) Select FLOW DATA option on the Diagnostic Software.
   Enter: BERT6.BIN for file name.
   Verify system displays Latched = 0x00
                         Unlatched=0x12
   Toggle Source from FIFO to BERT
   Toggle ENCODING to ENCODED
   Change Clock Register to 0x28   Check:_____

(6) Press RESTART on the FIREBIRD 6000   Check:_____

(7) Wait 1 minute.   Check:_____

(8) Record: Bit errors:_____ BLOCKS_____. If Bit errors NON_ZERO
   or SYNC LOST light ON, then test FAILED.   Check:_____
Circle:PASS/FAIL

(9) Patch A2TLM to BS#1 S0 IN.   Check:_____

(10)Press RESTART on FIREBIRD 6000.   Check:_____

(11)Wait 1 minute.   Check:_____

(12)Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
   or SYNC LOST light ON, then test FAILED.   Check:_____
Circle:PASS/FAIL

(13)Patch B1TLM to BS#1 S0 IN   Check:_____

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(14) Press RESTART on FIREBIRD 6000   Check:_____

(15) Wait 1 minute.   Check:_____

(16) Record: Bit errors:_____ Blocks:_____ If Bit errors NON-ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                      Circle:PASS/FAIL

(17) Patch B2TLM to BS#1 S0 IN.   Check:_____

(18) Press RESTART on FIREBIRD 6000.   Check:_____

(19) Wait 1 minute.   Check:_____

(20) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                      Circle:PASS/FAIL

3.4 BERT ENCODED 1KHZ PCMA Test

(1) Enter 132 on bit sync key-pad to configure bit sync as follows:
        Data Rate: 2Kbps (symbol rate)
        Input code: NRZ-L
        FEC Code:BPSK-D
        Rate: ½
                                                                      Check:_____

(2) Patch A1TLM to BS#1 S0 IN   Check:_____

(3) Change Clock Register to 0xC6   Check:_____

(4) Press RESTART on the FIREBIRD 6000   Check:_____

(5) Wait 1 minute.   Check:_____

(6) Record: Bit errors:_____ Blocks:_____. If Bit errors NON_ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                      Circle:PASS/FAIL

(7) Patch A2TLM to BS#1 S0 IN.   Check:_____

(8) Press RESTART on FIREBIRD 6000.   Check:_____

(9) Wait 1 minute.   Check:_____

(10) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                      Circle:PASS/FAIL

(11) Patch B1TLM to BS#1 S0 IN   Check:_____

(12) Press RESTART on FIREBIRD 6000   Check:_____

(13) Wait 1 minute.   Check:_____

(14) Record: Bit errors:_____ Blocks:_____ If Bit errors NON-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                     Circle:PASS/FAIL

(15) Patch B2TLM to BS#1 S0 IN.   Check:_____

(16) Press RESTART on FIREBIRD 6000.   Check:_____

(17) Wait 1 minute.   Check:_____

(18) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                     Circle:PASS/FAIL

3.5 BERT UNENCODED 1KHZ PCMA Test

(1) Enter 133 on bit sync key-pad to configure bit sync as follows:
    Data Rate: 1Kbps(bit rate)
    Input code: NRZ-L
    FEC Code:OFF
    Rate: ½
                                                  Check:_____

(2) Patch A1TLM to BS#1 S0 IN   Check:_____

(3) Toggle ENCODING to RAW.   Check:_____

(4) Press RESTART on the FIREBIRD 6000   Check:_____

(5) Wait 1 minute.   Check:_____

(6) Record: Bit errors:_____ Blocks:_____. If Bit errors NON_ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                     Circle:PASS/FAIL

(7) Patch A2TLM to BS#1 S0 IN.   Check:_____

(8) Press RESTART on FIREBIRD 6000.   Check:_____

(9) Wait 1 minute.   Check:_____

(10) Record: Bit errors:_____ Blocks_____. If Bit errors Non-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                      Circle:PASS/FAIL

(11) Patch B1TLM to BS#1 S0 IN   Check:_____

(12) Press RESTART on FIREBIRD 6000   Check:_____

(13) Wait 1 minute.   Check:_____

(14) Record: Bit errors:_____ Blocks:_____ If Bit errors NON-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____

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Circle:PASS/FAIL

(15)Patch B2TLM to BS#1 S0 IN.   Check:_____

(16)Press RESTART on FIREBIRD 6000.   Check:_____

(17)Wait 1 minute.   Check:_____

(18)Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
   or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                 Circle:PASS/FAIL

3.6 BERT UNENCODED 150KHZ PCMA

(1) Enter 131 on bit sync key-pad to configure bit sync as follows:
     Data Rate: 150Kbps(bit rate)
     Input code: NRZ-L
     FEC Code:OFF
     Rate: ½
                                                                 Check:_____

(2) Patch A1TLM to BS#1 S0 IN   Check:_____

(3) Change Clock Register to 0x28   Check:_____

(4) Press RESTART on the FIREBIRD 6000   Check:_____

(5) Wait 1 minute.   Check:_____

(6) Record: Bit errors:_____ Blocks:_____. If Bit errors NON_ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                 Circle:PASS/FAIL

(7) Patch A2TLM to BS#1 S0 IN.   Check:_____

(8) Press RESTART on FIREBIRD 6000.   Check:_____

(9) Wait 1 minute.   Check:_____

(10)Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
   or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                 Circle:PASS/FAIL

(11)Patch B1TLM to BS#1 S0 IN   Check:_____

(12)Press RESTART on FIREBIRD 6000   Check:_____

(13)Wait 1 minute.   Check:_____

(14)Record: Bit errors:_____ Blocks:_____ If Bit errors NON-ZERO
   or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                 Circle:PASS/FAIL

(15)Patch B2TLM to BS#1 S0 IN.   Check:_____

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(16) Press RESTART on FIREBIRD 6000.   Check:_____

(17) Wait 1 minute.   Check:_____

(18) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                       Circle:PASS/FAIL

3.7 BERT ENCODED 150KHZ PCMB Test

(1) Exit/Quit the Flow data section of the Diagnostic software   Check:_____

(2) Verify that PCM Discrete Deck A is selected by Reading I/O Port 0x01 and
    noting that msb is 0. If the msb is not zero, the test failed.   Check:_____
                                                                       Circle:PASS/FAIL

(3) Generate PCM-B Discrete Deck Select pulse command   Check:_____

(4) Verify that PCM Discrete Deck B is selected by Reading I/O Port 0x01 and
    noting that the msb is 1. If the msb is not 1, the test failed. Reg Value:_____Check:_____
                                                                       Circle:PASS/FAIL

(5) Press RESTART on the FIREBIRD.   Check:_____

(6) Wait 30 seconds   Check:_____

(7) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                       Circle:PASS/FAIL

(8) Enter 130 on bit sync key-pad to configure bit sync as follows:
        Data Rate: 300Kbps(symbol rate)
        Input code: NRZ-L
        FEC Code:BPSK-D
        Rate: ½
                                                                       Check:_____

(9) Patch A1TLM to BS#1 S0 IN   Check:_____

(10) Select FLOW DATA option on the Diagnostic Software.
    Enter: BERT6.BIN for file name.
        Verify Unlatched status =0x92
                Latched status = 0x80
    Toggle Source from FIFO to BERT
    Toggle ENCODING to ENCODING
    Change Clock Register to 0x28   Check:_____

(11) Press RESTART on the FIREBIRD 6000   Check:_____

(12) Wait 1 minute.   Check:_____

(13) Record: Bit errors:_____ Blocks:_____. If Bit errors NON_ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                       Circle:PASS/FAIL

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(14) Patch A2TLM to BS#1 S0 IN.   Check:_____

(15) Press RESTART on FIREBIRD 6000.   Check:_____

(16) Wait 1 minute.   Check:_____

(17) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                   Circle:PASS/FAIL

(18) Patch B1TLM to BS#1 S0 IN   Check:_____

(19) Press RESTART on FIREBIRD 6000   Check:_____

(20) Wait 1 minute.   Check:_____

(21) Record: Bit errors:_____ Blocks:_____ If Bit errors NON-ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                   Circle:PASS/FAIL

(22) Patch B2TLM to BS#1 S0 IN.   Check:_____

(23) Press RESTART on FIREBIRD 6000.   Check:_____

(24) Wait 1 minute.   Check:_____

(25) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                   Circle:PASS/FAIL

3.8 BERT ENCODED 1KHZ PCMB Test

(1) Enter 132 on bit sync key-pad to configure bit sync as follows:
        Data Rate: 2Kbps(symbol rate)
        Input code: NRZ-L
        FEC Code:BPSK-D
        Rate: ½
                                                                   Check:_____

(2) Patch A1TLM to BS#1 S0 IN   Check:_____

(3) Change Clock Register to 0xC6   Check:_____

(4) Press RESTART on the FIREBIRD 6000   Check:_____

(5) Wait 1 minute.   Check:_____

(6) Record: Bit errors:_____ Blocks:_____. If Bit errors NON_ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                   Circle:PASS/FAIL

(7) Patch A2TLM to BS#1 S0 IN.   Check:_____

(8) Press RESTART on FIREBIRD 6000.   Check:_____

(9) Wait 1 minute.   Check:_____

(10)Record: Bit errors:_____ Blocks:_____. If Block Errror NON-ZERO
or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                                  Circle:PASS/FAIL

(11)Patch B1TLM to BS#1 S0 IN   Check:_____

(12)Press RESTART on FIREBIRD 6000   Check:_____

(13)Wait 1 minute.   Check:_____

(14)Record: Bit errors:_____ Blocks:_____ If Bit errors NON-ZERO
or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                                  Circle:PASS/FAIL

(15)Patch B2TLM to BS#1 S0 IN.   Check:_____

(16)Press RESTART on FIREBIRD 6000.   Check:_____

(17)Wait 1 minute.   Check:_____

(18)Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                                  Circle:PASS/FAIL

3.9 BERT UNENCODED 1KHZ PCMB Test

(1) Enter 133 on bit sync key-pad to configure bit sync as follows:
        Data Rate: 1Kbps(bit rate)
        Input code: NRZ-L
        FEC Code:OFF
        Rate: ½
                                                                                  Check:_____

(2) Patch A1TLM to BS#1 S0 IN   Check:_____

(3) Toggle Encoding to RAW   Check:_____

(4) Press RESTART on the FIREBIRD 6000   Check:_____

(5) Wait 1 minute.   Check:_____

(6) Record: Bit errors:_____ Blocks:_____. If Bit errors NON_ZERO
        or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                                  Circle:PASS/FAIL

(7) Patch A2TLM to BS#1 S0 IN.   Check:_____

(8) Press RESTART on FIREBIRD 6000.   Check:_____

(9) Wait 1 minute.   Check:_____

(10)Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
        or SYNC LOST light ON, then test FAILED.   Check:_____

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Circle:PASS/FAIL

(11)Patch B1TLM to BS#1 S0 IN   Check:_____

(12)Press RESTART on FIREBIRD 6000   Check:_____

(13)Wait 1 minute.   Check:_____

(14)Record: Bit errors:_____ Blocks:_____ If Bit errors NON-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                  Circle:PASS/FAIL

(15)Patch B2TLM to BS#1 S0 IN.   Check:_____

(16)Press RESTART on FIREBIRD 6000.   Check:_____

(17)Wait 1 minute.   Check:_____

(18)Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                  Circle:PASS/FAIL

3.10 BERT UNENCODED 150KHZ PCMB Test

(1) Enter 131 on bit sync key-pad to configure bit sync as follows:
    Data Rate: 150Kbps(bit rate)
    Input code: NRZ-L
    FEC Code:OFF
    Rate: ½
                                                                  Check:_____

(2) Patch A1TLM to BS#1 S0 IN   Check:_____

(3) Change Clock Register to 0x28   Check:_____

(4) Press RESTART on the FIREBIRD 6000   Check:_____

(5) Wait 1 minute.   Check:_____

(6) Record: Bit errors:_____ Blocks:_____. If Bit errors NON_ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                  Circle:PASS/FAIL

(7) Patch A2TLM to BS#1 S0 IN.   Check:_____

(8) Press RESTART on FIREBIRD 6000.   Check:_____

(9) Wait 1 minute.   Check:_____

(10)Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                  Circle:PASS/FAIL

(11)Patch B1TLM to BS#1 S0 IN   Check:_____

(12) Press RESTART on FIREBIRD 6000   Check:_____

(13) Wait 1 minute.   Check:_____

(14) Record: Bit errors:_____ Blocks:_____ If Bit errors NON-ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
                                                              Circle:PASS/FAIL

(15) Patch B2TLM to BS#1 S0 IN.   Check:_____

(16) Press RESTART on FIREBIRD 6000.   Check:_____

(17) Wait 1 minute.   Check:_____

(18) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
                                                              Circle:PASS/FAIL

3.11 FIFO ENCODED150KHZ PCMA and Software Reset In PCM-BTest

(1) Quit/Exit the Flow Data section of the Diagnostic Code   Check:_____

(2) Verify that PCM-B discrete deck is selected by Reading I/O Port 0x01 and
     Noting that the msb is 1. If the msb is not 1, the test failed. Reg Value:_____Check:_____
                                                              Circle:PASS/FAIL

(3) Read clock register by Reading I/O port 0x02. Record contents:_____   Check:_____

(4) Read configuration register by Reading I/O Port 0x03. Record contents_____
                                                              Check:_____

(5) Read Latched FIFO Status by Reading I/O Port 0x00. Record contents:_____
                                                              Check:_____

(6) Read Unlatched FIFO Status by Reading I/O Port 0x01. Record contents_____
                                                              Check:_____

(7) Issue SOFT RESET.   Check:_____

(8) Read Clock Register by Reading I/O Port 0x02. Record contents:_____
     If different from Step 3 test failed.   Check:_____
                                                              Circle PASS/FAIL

(9) Read configuration register by Reading I/O Port 0x03. Record contents:_____
     If different from Step 4, test failed.   Check:_____
                                                              CirclePASS/FAIL

(10) Read Latched FIFO Status by Reading I/O Port 0x00. Record contents._____
     If not 0x80 test FAILED.   Check:_____
                                                              Circle PASS/FAIL

(11) Read Unlatched FIFO Status by Reading I/O Port 0x01. Record Contents:_____
     Value must equal 0x89 or test failed.   Check:_____
                                                              Circle PASS?FAIL

(12) Generate PCM-A Discrete Deck Select using HP pulse generator   Check:_____

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(13) Verify that PCM Discrete Deck A is selected by Reading I/O Port 0x01 and
noting that the msb is zero. If the msb is not zero, the test failed. Reg Value:_____ Check:_____
Circl:PASS/FAIL

(14) Press RESTART on FIREBIRD 6000.   Check:_____

(15) Wait 30 seconds.   Check:_____

(16) Record: Bit errors:_____ Blocks:_____ If Bit errors NONZERO,
or SYNC LOST light ON, then test FAILED   Check:_____
Circle:PASS/PAIL

(17) Enter 130 on bit sync key-pad to configure bit sync as follows:
     Data Rate: 300Kbps(symbol rate)
     Input code: NRZ-L
     FEC Code:BPSK-D
     Rate: ½
                                                       Check:_____

(18) Configure Firebird 6000 for BERT Pattern 63 and press RESTART   Check:_____

(19) Patch A1TLM to BS#1 S0 IN   Check:_____

(20) Select FLOW DATA option on the Diagnostic Software.
Enter: BERT6.BIN for file name.
Toggle ENCODING to ENCODING
Toggle Source to FIFO
Change Clock Register to 0x28   Check:_____

(21) Press RESTART on the FIREBIRD 6000   Check:_____

(22) Wait 1 minute.   Check:_____

(23) Record: Bit errors:_____ Blocks:_____. If Bit errors NON_ZERO
or SYNC LOST light ON, then test FAILED.   Check:_____
Circle:PASS/FAIL

(24) Patch A2TLM to BS#1 S0 IN.   Check:_____

(25) Press RESTART on FIREBIRD 6000.   Check:_____

(26) Wait 1 minute.   Check:_____

(27) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
or SYNC LOST light ON, then test FAILED.   Check:_____
Circle:PASS/FAIL

(28) Patch B1TLM to BS#1 S0 IN   Check:_____

(29) Press RESTART on FIREBIRD 6000   Check:_____

(30) Wait 1 minute.   Check:_____

(31) Record: Bit errors:_____ Blocks:_____ If Bit errors NON-ZERO

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or SYNC LOST light ON, then test FAILED.   Check:_____
                      Circle:PASS/FAIL

(32)Patch B2TLM to BS#1 S0 IN.   Check:_____

(33)Press RESTART on FIREBIRD 6000.   Check:_____

(34)Wait 1 minute.   Check:_____

(35)Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                      Circle:PASS/FAIL

3.12 FIFO DATA ENCODED 1KHZ PCMA test

(1) Enter 132 on bit sync key-pad to configure bit sync as follows:
       Data Rate: 2Kbps(symbol rate)
       Input code: NRZ-L
       FEC Code:BPSK-D
       Rate: ½
                      Check:_____

(2) Patch A1TLM to BS#1 S0 IN   Check:_____

(3) Change Clock Register to 0xC6.   Check:_____

(4) Press RESTART on the FIREBIRD 6000   Check:_____

(5) Wait 1 minute.   Check:_____

(6) Record: Bit errors:_____ Blocks:_____. If Bit errors NON_ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                      Circle:PASS/FAIL

(7) Patch A2TLM to BS#1 S0 IN.   Check:_____

(8) Press RESTART on FIREBIRD 6000.   Check:_____

(9) Wait 1 minute.   Check:_____

(10)Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                      Circle:PASS/FAIL

(11)Patch B1TLM to BS#1 S0 IN   Check:_____

(12)Press RESTART on FIREBIRD 6000   Check:_____

(13)Wait 1 minute.   Check:_____

(14)Record: Bit errors:_____ Blocks:_____ If Bit errors NON-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                      Circle:PASS/FAIL

(15)Patch B2TLM to BS#1 S0 IN.   Check:_____

(16) Press RESTART on FIREBIRD 6000.   Check:_____

(17) Wait 1 minute.   Check:_____

(18) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
        or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                        Circle:PASS/FAIL

3.13 FIFO DATA ENCODED 150KHZ PCMB Test

(1) Quit/Exit Flow Data section of diagnostic software.   Check:_____

(2) Verify that PCM-A discrete deck is selected by Reading I/O Port 0x01 and
      Noting that the msb is 0. If the msb is not zero, the test failed. Reg Value:_____Check:_____
                                                                        Circle:PASS/FAIL

(3) Generate PCM-B Discrete Deck Select using HP pulse generator   Check:_____

(4) Verify that PCM Discrete Deck B is selected by Inputting Port 0x01 and
      noting that the msb is 1. If the msb is not 1, the test failed.. Reg Value:_____Check:_____
                                                                        Circle:PASS/FAIL

(5) Enter 130 on bit sync key-pad to configure bit sync as follows:
        Data Rate: 300Kbps(symbol rate)
        Input code: NRZ-L
        FEC Code:BPSK-D
        Rate: ½
                                                                        Check:_____

(6) Patch A1TLM to BS#1 S0 IN   Check:_____

(36) Select FLOW DATA option on the Diagnostic Software.
      Enter: BERT6.BIN for file name.
      Toggle ENCODING to ENCODING
      Toggle Source to FIFO
      Change Clock Register to 0x28   Check:_____

(7) Press RESTART on the FIREBIRD 6000   Check:_____

(8) Wait 1 minute.   Check:_____

(9) Record: Bit errors:_____ Blocks:_____. If Bit errors NON_ZERO
      or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                        Circle:PASS/FAIL

(10) Patch A2TLM to BS#1 S0 IN.   Check:_____

(11) Press RESTART on FIREBIRD 6000.   Check:_____

(12) Wait 1 minute.   Check:_____

(13) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
      or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                        Circle:PASS/FAIL

(14) Patch B1TLM to BS#1 S0 IN   Check:_____

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(15) Press RESTART on FIREBIRD 6000   Check:_____

(16) Wait 1 minute.   Check:_____

(17) Record: Bit errors:_____ Blocks:_____ If Bit errors NON-ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
                                                          Circle:PASS/FAIL

(18) Patch B2TLM to BS#1 S0 IN.   Check:_____

(19) Press RESTART on FIREBIRD 6000.   Check:_____

(20) Wait 1 minute.   Check:_____

(21) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
                                                          Circle:PASS/FAIL

3.14 FIFO DATA ENCODED 1KHZ PCMB test

(1) Enter 132 on bit sync key-pad to configure bit sync as follows:
     Data Rate: 2Kbps(symbol rate)
     Input code: NRZ-L
     FEC Code:BPSK-D
     Rate: ½
                                                            Check:_____

(2) Patch A1TLM to BS#1 S0 IN   Check:_____

(3) Change Clock Register to 0xC6   Check:_____

(4) Press RESTART on the FIREBIRD 6000   Check:_____

(5) Wait 1 minute.   Check:_____

(6) Record: Bit errors:_____ Blocks:_____. If Bit errors NON_ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
                                                          Circle:PASS/FAIL

(7) Patch A2TLM to BS#1 S0 IN.   Check:_____

(8) Press RESTART on FIREBIRD 6000.   Check:_____

(9) Wait 1 minute.   Check:_____

(10) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
                                                          Circle:PASS/FAIL

(11) Patch B1TLM to BS#1 S0 IN   Check:_____

(12) Press RESTART on FIREBIRD 6000   Check:_____

(13) Wait 1 minute.   Check:_____

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(14) Record: Bit errors:_____ Blocks:_____ If Bit errors NON-ZERO
or SYNC LOST light ON, then test FAILED.   Check:_____
Circle:PASS/FAIL

(15) Patch B2 TLM to BS#1 S0 IN.   Check:_____

(16) Press RESTART on FIREBIRD 6000.   Check:_____

(17) Wait 1 minute.   Check:_____

(18) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
or SYNC LOST light ON, then test FAILED.   Check:_____
Circle:PASS/FAIL

3.15 FIFO ENCODED INTERMEDIATE DATA RATE PCMA Test

(1) Quit/Exit Flow Data portion of Diagnostic Software.   Check:_____

(2) Verify that PCM-B discrete deck is selected by Reading I/O Port 0x01 and
Noting that the msb is 1. If the msb is not 1, the test failed. Reg Value:_____Check:_____
Circle:PASS/FAIL

(3) Generate PCM-A Discrete Deck Select using HP pulse generator   Check:_____

(4) Verify that PCM Discrete Deck A is selected by Reading I/O Port 0x01 and
noting that the msb is zero. If the msb is not zero, the test failed. Reg Value:_____Check:_____
Circle:PASS/FAIL

(5) Enter 134 on bit sync key-pad to configure bit sync as follows:
Data Rate: 100Kbps(symbol rate)
Input code: NRZ-L
FEC Code:BPSK-D
Rate: ½
Check:_____

(6) Patch A1 TLM to BS#1 S0 IN   Check:_____

(7) Select FLOW DATA option on the Diagnostic Software.
Enter: BERT 6.BIN for file name.
Toggle ENCODING to ENCODING
Toggle Source to FIFO
Change Clock Register to 0x4C   Check:_____

(8) Press RESTART on the FIREBIRD 6000   Check:_____

(9) Wait 1 minute.   Check:_____

(10) Record: Bit errors:_____ Blocks:_____. If Bit errors NON_ZERO
or SYNC LOST light ON, then test FAILED.   Check:_____
Circle:PASS/FAIL

(11) Patch A2 TLM to BS#1 S0 IN.   Check:_____

(12) Press RESTART on FIREBIRD 6000.   Check:_____

(13) Wait 1 minute.   Check:_____

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(14) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                            Circle:PASS/FAIL

(15) Patch B1 TLM to BS#1 S0 IN   Check:_____

(16) Press RESTART on FIREBIRD 6000   Check:_____

(17) Wait 1 minute.   Check:_____

(18) Record: Bit errors:_____ Blocks:_____ If Bit errors NON-ZERO
or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                            Circle:PASS/FAIL

(19) Patch B2 TLM to BS#1 S0 IN.   Check:_____

(20) Press RESTART on FIREBIRD 6000.   Check:_____

(21) Wait 1 minute.   Check:_____

(22) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                            Circle:PASS/FAIL

3.16 FIFO UNENCODED INTERMEDIATE DATA RATE PCMA Test

(1) Enter 135 on bit sync key-pad to configure bit sync as follows:
      Data Rate: 50Kbps(bit rate)
      Input code: NRZ-L
      FEC Code:OFF
      Rate: ½
                                                                            Check:_____

(2) Patch A1 TLM to BS#1 S0 IN   Check:_____

(3) Toggle ENCODING to RAW   Check:_____

(4) Press RESTART on the FIREBIRD 6000   Check:_____

(5) Wait 1 minute.   Check:_____

(6) Record: Bit errors:_____ Blocks:_____. If Bit errors NON_ZERO
or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                            Circle:PASS/FAIL

(7) Patch A2 TLM to BS#1 S0 IN.   Check:_____

(8) Press RESTART on FIREBIRD 6000.   Check:_____

(9) Wait 1 minute.   Check:_____

(10) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                            Circle:PASS/FAIL

(11) Patch B1TLM to BS#1 S0 IN   Check:_____

(12) Press RESTART on FIREBIRD 6000   Check:_____

(13) Wait 1 minute.   Check:_____

(14) Record: Bit errors:_____ Blocks:_____ If Bit errors NON-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                  Circle:PASS/FAIL

(15) Patch B2TLM to BS#1 S0 IN.   Check:_____

(16) Press RESTART on FIREBIRD 6000.   Check:_____

(17) Wait 1 minute.   Check:_____

(18) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                  Circle:PASS/FAIL

3.17 FIFO DATA ENCODED INTERMEDIATE DATA RATE PCMB and Soft Reset In PCMA Test

(1) Change Clock Register to 0x00. (Stop Clock).   Check:_____

(2) Quit/Exit the Flow Data section of the Diagnostic Code   Check:_____

(3) Verify that PCM-A discrete deck is selected by Reading I/O Port 0x01 and
    Noting that the msb is 0. If the msb is not zero, the test failed. Reg Value:_____ Check:_____
                                                                    Circle:PASS/FAIL

(4) Read clock register by Reading I/O port 0x02. Record contents:_____   Check:_____

(5) Read configuration register by Reading I/O Port 0x03. Record contents_____
                                                                     Check:_____

(6) Read Latched FIFO Status by Reading I/O Port 0x00. Record contents:_____
                                                                     Check:_____

(7) Read Unlatched FIFO Status by Reading I/O Port 0x01. Record contents_____
                                                                     Check:_____

(8) Issue SOFT RESET.   Check:_____

(9) Read Clock Register by Reading I/O Port 0x02. Record contents:_____
    If different from Step 4 test failed.   Check:_____
                                                                     Circle PASS/FAIL

(10) Read configuration register by Reading I/O Port 0x03. Record contents:_____
    If different from Step 5, test failed.   Check:_____
                                                                     CirclePASS/FAIL

(11) Read Latched FIFO Status by Reading I/O Port 0x00. Record contents._____
    If not 0x00 then test FAILED.   Check:_____
                                                                     Circle PASS/FAIL

`

(12) Read Unlatched FIFO Status by Reading I/O Port 0x01. Record Contents:_____
    Value must equal 0x09 or test failed.   Check:_____
                                                       Circle PASS?FAIL

(13) Generate PCM-B Discrete Deck Select using HP pulse generator   Check:_____

(14) Verify that PCM Discrete Deck B is selected by Reading I/O Port 0x01 and
    noting that the msb is 1. If the msb is not 1, the test failed. Reg Value:_____Check:_____
                                                     Circle:PASS/FAIL

(15) Resume clock by Outputting to I/O Port 0x02 0x4c.
         Check:_____

(16) Issue SOFT RESET.   Check:_____

(17) Read Clock Register to verify it did not change by Reading I/O Port 0x02.
    Verify contents = 0x4c. Reg Value:_____. If not = 0x4c, then test
    FAILED   Check:_____
                                                 Circle: PASS/FAIL

(18) Enter 134 on bit sync key-pad to configure bit sync as follows:
    Data Rate: 100Kbps(symbol rate)
    Input code: NRZ-L
    FEC Code:BPSK-D
    Rate: ½
                                           Check:_____

(19) Patch A1TLM to BS#1 S0 IN   Check:_____

(20) Select FLOW DATA option on the Diagnostic Software.
    Enter: BERT6.BIN for file name.
    Toggle ENCODING to ENCODING
    Toggle Source to FIFO
    Change Clock Register to 0x4C   Check:_____

(21) Press RESTART on the FIREBIRD 6000   Check:_____

(22) Wait 1 minute.   Check:_____

(23) Record: Bit errors:_____   Blocks:_____. If Bit errors NON_ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                Circle:PASS/FAIL

(24) Patch A2TLM to BS#1 S0 IN.   Check:_____

(25) Press RESTART on FIREBIRD 6000.   Check:_____

(26) Wait 1 minute.   Check:_____

(27) Record: Bit errors:_____   Blocks:_____. If Bit errors NON-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                Circle:PASS/FAIL

(28) Patch B1TLM to BS#1 S0 IN   Check:_____

(29) Press RESTART on FIREBIRD 6000   Check:_____

`

(30) Wait 1 minute.   Check:_____

(31) Record: Bit errors:_____ Blocks:_____ If Bit errors NON-ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                                Circle:PASS/FAIL

(32) Patch B2TLM to BS#1 S0 IN.   Check:_____

(33) Press RESTART on FIREBIRD 6000.   Check:_____

(34) Wait 1 minute.   Check:_____

(35) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                                Circle:PASS/FAIL

3.18 FIFO DATA UNENCODED INTERMEDIATE DATA RATE PCMB test

(1) Enter 135 on bit sync key-pad to configure bit sync as follows:
     Data Rate: 50Kbps(bit rate)
     Input code: NRZ-L
     FEC Code:OFF
     Rate: ½
                                                                                Check:_____

(2) Patch A1TLM to BS#1 S0 IN   Check:_____

(3) Toggle ENCODED to RAW   Check:_____

(4) Press RESTART on the FIREBIRD 6000   Check:_____

(5) Wait 1 minute.   Check:_____

(6) Record: Bit errors:_____ Blocks_____. If Bit errors NON_ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                                Circle:PASS/FAIL

(7) Patch A2TLM to BS#1 S0 IN.   Check:_____

(8) Press RESTART on FIREBIRD 6000.   Check:_____

(9) Wait 1 minute.   Check:_____

(10) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                                Circle:PASS/FAIL

(11) Patch B1TLM to BS#1 S0 IN   Check:_____

(12) Press RESTART on FIREBIRD 6000   Check:_____

(13) Wait 1 minute.   Check:_____

(14) Record: Bit errors:_____ Blocks:_____ If Bit errors NON-ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____

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`

Circle:PASS/FAIL

(15)Patch B2TLM to BS#1 S0 IN.   Check:_____

(16)Press RESTART on FIREBIRD 6000.   Check:_____

(17)Wait 1 minute.   Check:_____

(18)Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                                              Circle:PASS/FAIL

3.19 Verify TDI Test Points

(1) Toggle Encoding to ENCODED to demonstrate that the TPs output RAW data.Check:_____

(2) Set the clock register to 0x28   Check:_____

(3) Patch A1xCLK to the frequency counter. Verify the counter reads
    150000 +/- 150 counts. Record counts:_____
      Check:_____

(4) Patch A2xClk to the frequency counter.   Verify the counter reads
    300000 +/- 300 counts. Record counts:_____   Check:_____

(5) Patch B1xCLK to frequency counter. Verify the counter reads
    150000 +/- 150 counts. Record counts:_____   Check:_____

(6) Patch B2xCLK to the frequency counter. Verify the counter reads
    300000 +/- 300 counts. Record counts:_____   Check:_____

(7) Enter 136 on bit sync key-pad to configure the bit sync as follows:
    Data Rate: 150Kbps(bit rate)
    Input Code: NRZ-M
    FEC Code:OFF
                                                       Check:_____

(8) Patch NRZ-M A TP to BS#1 S0 IN   Check:_____

(9) Press RESTART on FIREBIRD 6000   Check:_____

(10)Wait 1 minute.   Check:_____

(11)Record: Bit errors:_____   Blocks:_____. If Bit errors NON-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____
                                                          Circle:PASS/FAIL

(12)Patch NRZ-M B TP to BS#1 S0 IN   Check:_____

(13)Press RESTART on FIREBIRD 6000   Check:_____

(14)Wait 1 minute.   Check:_____

(15)Record: Bit errors:_____   Blocks:_____. If Bit errors NON-ZERO
    or SYNC LOST light ON, then test FAILED.   Check:_____

`

Circle PASS/FAIL

(16) Enter 137 on bit sync key-pad to configure the bit sync as follows:
     Data Rate: 150Kbps(bit rate)
     Input Code: BiO-L
     FEC Code:OFF

          Check:_____

(17) Patch BiO-L A TP to BS#1 S0 IN   Check:_____

(18) Press RESTART on FIREBIRD 6000   Check:_____

(19) Wait 1 minute.   Check:_____

(20) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
              Circle:PASS/FAIL

(21) Patch BiO-L B TP to BS#1 S0 IN   Check:_____

(22) Press RESTART on FIREBIRD 6000   Check:_____

(23) Wait 1 minute.   Check:_____

(24) Record: Bit errors:_____ Blocks:_____. If Bit errors NON-ZERO
     or SYNC LOST light ON, then test FAILED.   Check:_____
              Circle:PASS/FAIL

4. Declaration of Test Results

If there where no failures encountered during the execution of this test procedure that were not induced by procedural errors or GSE failures, then the TDI board in ULDB mode PASSES the TDI ULDB MODE SFT.

The test conductors and TDI system engineer declare that:

TDI board   Serial Number:_____
          FPGA Signature Number:_____

PASSED/FAILED(Circle One) the TDI ULDB MODE SFT on _____(date)
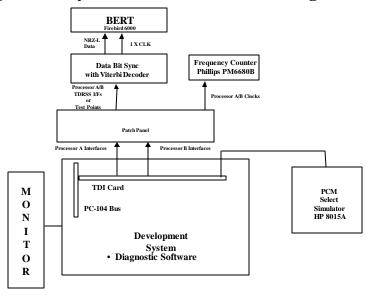
Test Conductor #1_____

Test Conductor #2_____

TDI Systems Engineer:_____

Figure 2.4 System Functional Test Configuration